Software defined FPGA for parallel and low latency computing

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The domain we are working on:

- Hardware acceleration based on C to FPGA bitstream automatic synthesis

What we have:

- Open source tool for the High Level Synthesis named bambu (freely available at http://panda.dei.polimi.it)
- Developed with the help of several EU and ESA projects
- Supporting standard ANSI C and based on standard GCC
- Partially supporting OpenMP
- Supporting floating point customization
- Performances comparable with commercial tools
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In which domains we used such infrastructure:

- High frequency financial market data normalizer/provider (10G)
- Optimization of queries for graph-based databases
- Integration of parallel cores in Intel HARP infrastructure
- Crypto cores implementation/classification
- Predictable core generations for model-based space avionics

What we would like to do:

- Seamless debugging of sequential/parallel code for SW defined FPGA
- Extend parallel constructs support (pthread, OpenMP)
- Improving performance predictability for low latency applications